CLAIMS

What is claimed is:

1   1. An apparatus, comprising:

2   a direct memory access register adapted to hold a descriptor, said register comprising:

3   a command register comprising a compare enable bit and a branch enable bit;

4   a source address register;

5   a target address register; and

6   a descriptor address register.

1   2. An apparatus as in claim 1, wherein said compare enable bit is adapted to indicate a

2 comparison operation to be performed by said direct memory access controller based on said

3 source address register and said target address register.

1   3. An apparatus as in claim 1, wherein said branch enable bit is adapted to indicate a

2 branch operation to be performed by said direct memory access controller to access another

3 descriptor.

1   4. An apparatus as in claim 1, further comprising a control status register, said control

2 status register comprising a compare status bit.

1   5. An apparatus as in claim 4, wherein said branch enable bit is adapted to indicate a

2 branch operation to be performed by said direct memory access controller to access another

3 descriptor based on said compare status bit.

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1   6. A system, comprising:

2   a target;

3   a source;

4   a memory adapted to contain a first descriptor of a first type, a second descriptor of a

5   second type, a third descriptor of a third type, and a fourth descriptor of said first type;

6   a direct memory access controller coupled to said memory, said direct memory access

7   controller adapted to transfer data from said source to said target based on said first descriptor,

8   said direct memory access controller comprising a direct memory access register to hold said

9   first descriptor, said second descriptor, or said third descriptor, said direct memory access

10   register comprising a command register comprising a compare enable bit and a branch enable bit.

1   7. A system as in claim 6, said direct memory access register further comprising a source

2   address register and a target address register.

1   8. A system as in claim 7, wherein said compare enable bit is adapted to indicate a

2   comparison operation to be performed by said direct memory access controller based on said

3   source address register and said target address register.

1   9. A system as in claim 6, wherein said branch enable bit is adapted to indicate a branch

2   operation to be performed by said direct memory access controller to fetch said fourth descriptor

3   or said third descriptor from said memory.

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1   10. A system as in claim 9, wherein said first descriptor is adapted to indicate data

2   transfer by said direct memory access controller, and wherein said third descriptor is adapted to

3   indicate no data transfer by said direct memory access controller.

1   11. A system as in claim 6, said direct memory access controller further comprising a

2   control status register, said control status register comprising a compare status bit.

1   12. A system as in claim 11, wherein said branch enable bit is adapted to indicate a

2   branch operation to be performed by said direct memory access controller to fetch said fourth

3   descriptor or said third descriptor from said memory based on said compare status bit.

1   13. A system as in claim 11, wherein said direct memory access controller is adapted to

2   perform a comparison operation and a branch operation based on said branch enable bit, said

3   comparison enable bit, and said compare status bit.

1   14. A machine-readable medium that provides instructions, which when executed by a

2   computing platform, cause said computing platform to perform operations comprising a method

3   of:

4   fetching a first descriptor of a first type, said first descriptor identifying a first source and

5   a first target;

6   transferring a first data set over a direct memory access channel from said first source to

7   said first target based on said first descriptor;

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8   fetching a second descriptor of a second type, said second descriptor identifying a second

9   source, said second descriptor comprising comparison data;

10   fetching data from said second source identified by said second descriptor;

11   comparing said data fetched from said second source and said comparison data to obtain

12   a comparison result; and

13   fetching one of a fourth descriptor of said first type and a third descriptor of a third type

14   based on said comparison result.

1   15. A machine-readable medium as in claim 14, wherein said fourth descriptor is fetched

2   if said comparison result indicates said data fetched from said second source fails to match said

3   comparison data.

1   16. A machine-readable medium as in claim 14, wherein said third descriptor is fetched

2   if said comparison result indicates said data fetched from said second source matches said

3   comparison data.

1   17. A machine-readable medium as in claim 14, wherein said second descriptor

2   comprises a branch enable bit and a comparison enable bit, wherein said comparing data fetched

3   is based on said comparison enable bit in said second descriptor, and said fetching one of said

4   fourth descriptor and said third descriptor is based on said branch enable bit in said second

5   descriptor.

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1   18. A machine-readable medium as in claim 14, wherein said data fetched from said

2   second source comprises a transfer status indicator.

1   19. A method, comprising:

2   fetching a first descriptor of a first type, said first descriptor identifying a first source and

3   a first target;

4   transferring a first data set over a direct memory access channel from said first source to

5   said first target based on said first descriptor;

6   fetching a second descriptor of a second type, said second descriptor identifying a second

7   source, said second descriptor comprising comparison data;

8   fetching data from said second source identified by said second descriptor;

9   comparing said data fetched from said second source and said comparison data to obtain

10   a comparison result; and

11   fetching one of a fourth descriptor of said first type and a third descriptor of a third type

12   based on said comparison result.

1   20. A method as in claim 19, wherein said fourth descriptor is fetched if said comparison

2   result indicates said data fetched from said second source fails to match said comparison data.

1   21. A method as in claim 19, wherein said third descriptor is fetched if said comparison

2   result indicates said data fetched from said second source matches said comparison data.

1   22. A method as in claim 19, wherein said second descriptor comprises a branch enable

2   bit and a comparison enable bit, wherein said comparing data fetched is based on said

3   comparison enable bit in said second descriptor, and said fetching one of said fourth descriptor

4   and said third descriptor is based on said branch enable bit in said second descriptor.

1   23. A machine-readable medium as in claim 19, wherein said data fetched from said

2   second source comprises a transfer status indicator.